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FIG. 1
PRIOR ART

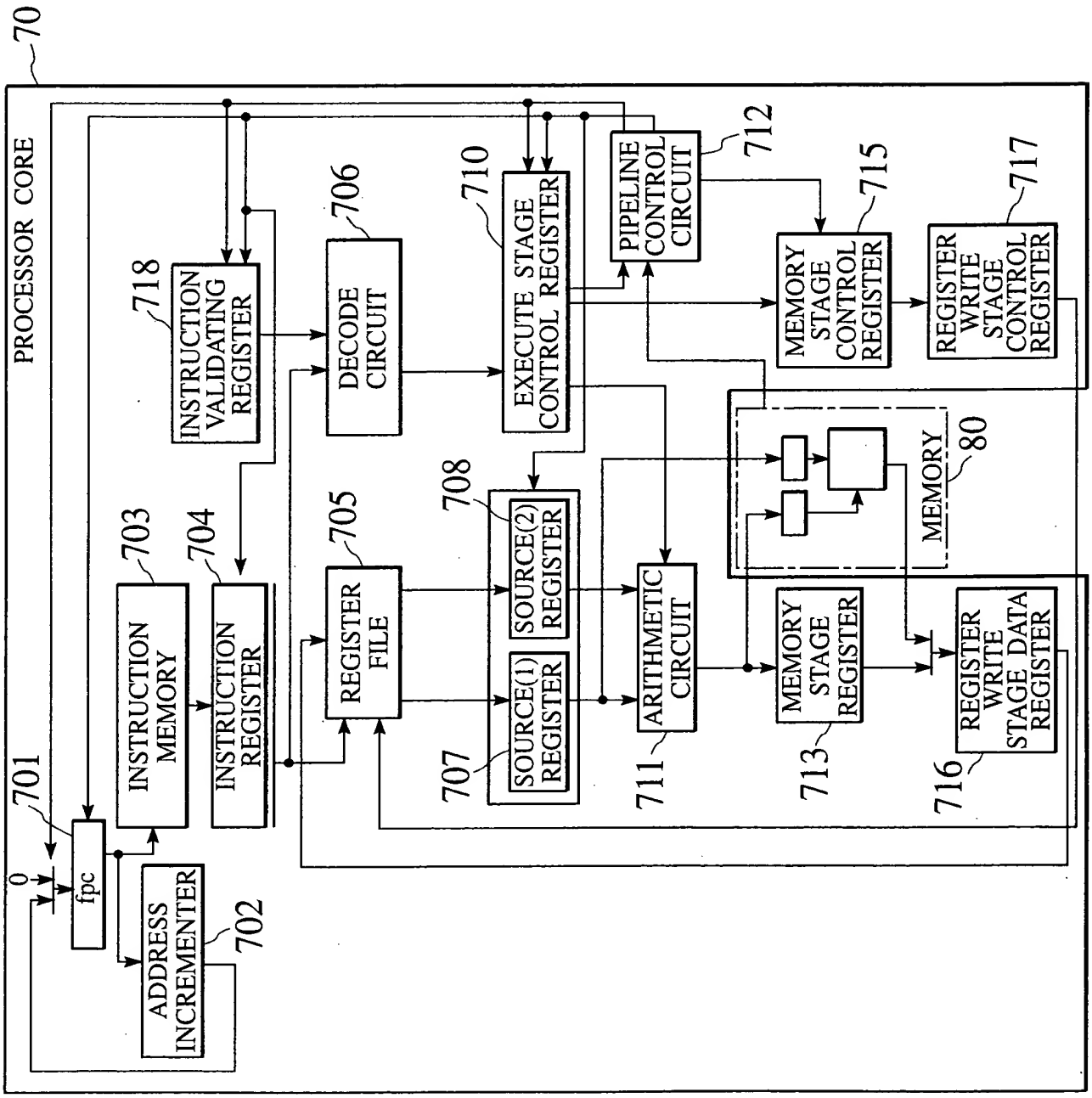


FIG. 2
PRIOR ART

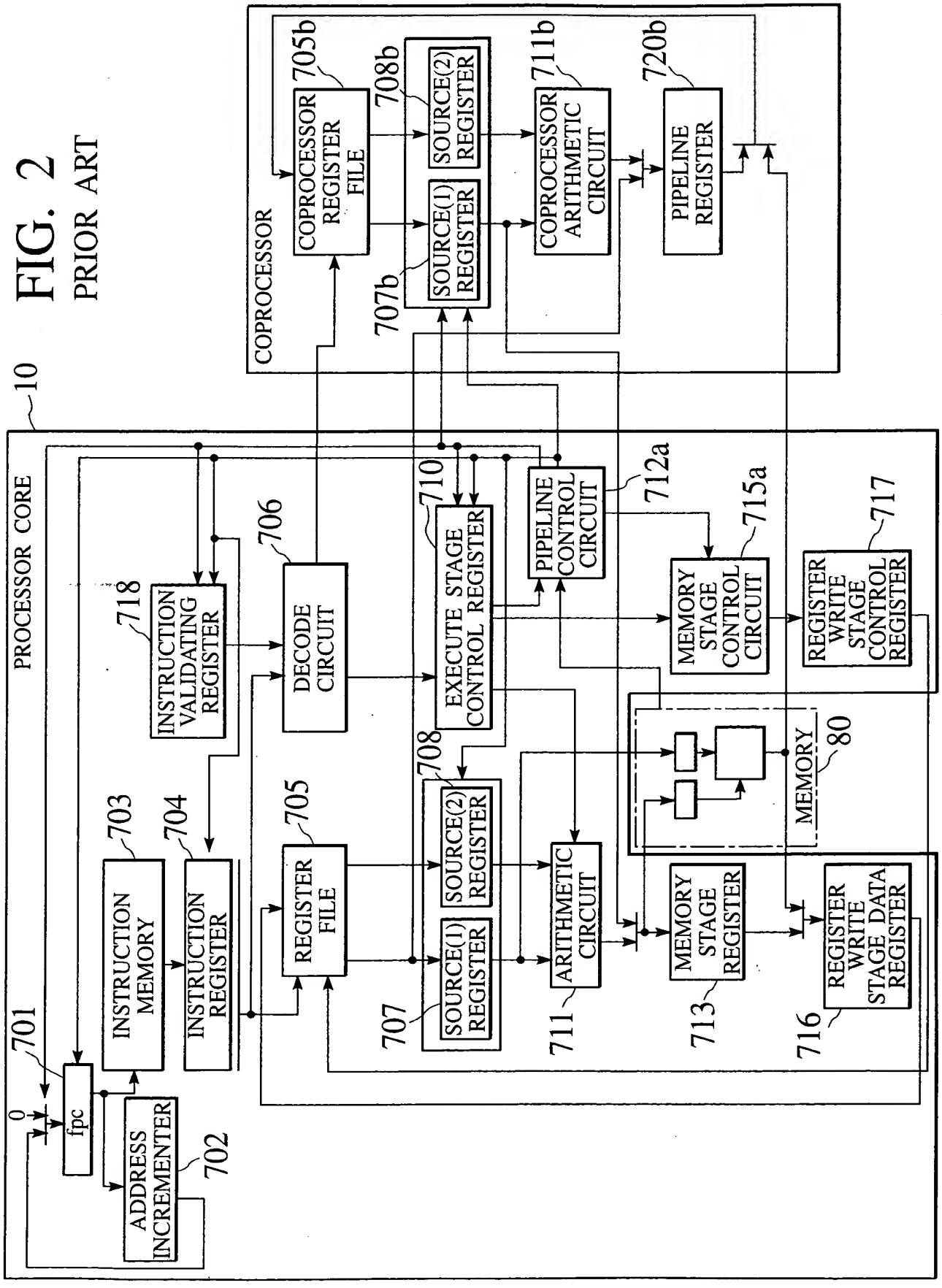


FIG. 3

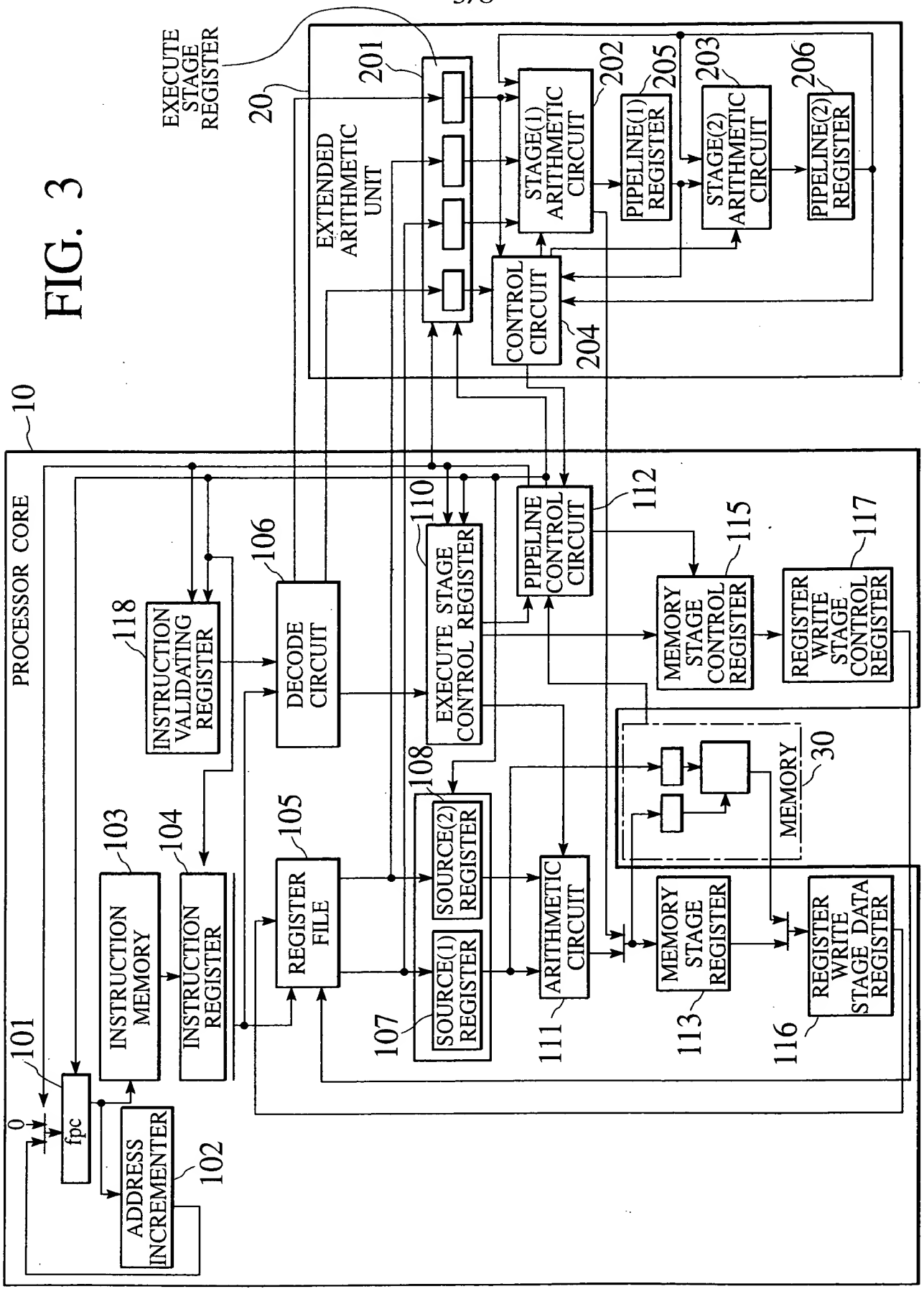
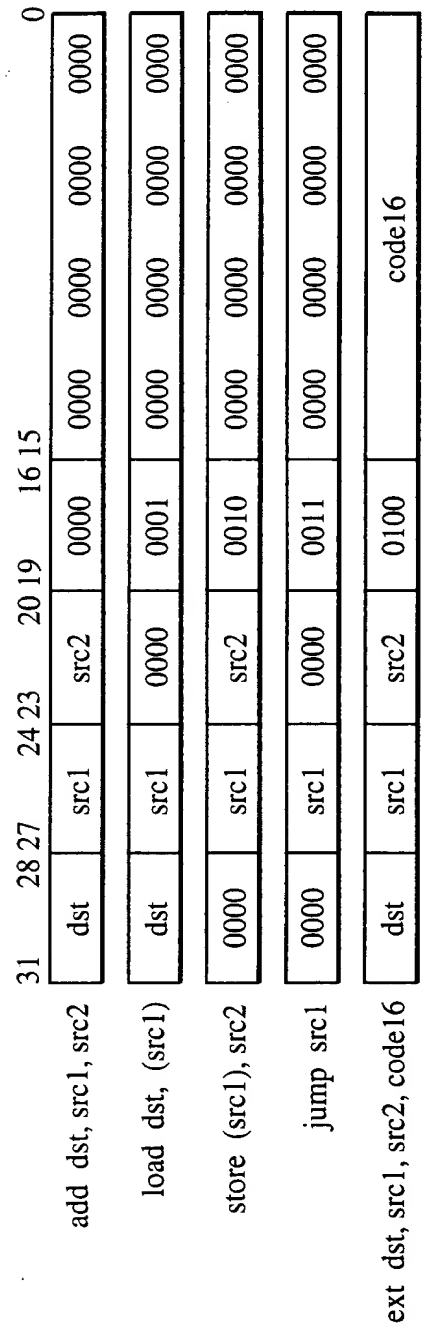

PROCESSOR CORE
10
EXTENDED ARITHMETIC UNIT
20
EXECUTE STAGE REGISTER
201
STAGE(1) ARITHMETIC CIRCUIT
202
PIPELINE(1) REGISTER
205
STAGE(2) ARITHMETIC CIRCUIT
203
PIPELINE(2) REGISTER
206
CONTROL CIRCUIT
204
PIPELINE CONTROL CIRCUIT
112
EXECUTE STAGE CONTROL REGISTER
110
MEMORY STAGE CONTROL REGISTER
115
REGISTER WRITE STAGE CONTROL REGISTER
117
INSTRUCTION VALIDATING REGISTER
118
DECODE CIRCUIT
106
INSTRUCTION MEMORY
103
INSTRUCTION REGISTER
104
REGISTER FILE
105
SOURCE(2) REGISTER
108
SOURCE(1) REGISTER
107
ARITHMETIC CIRCUIT
111
MEMORY
30
MEMORY STAGE REGISTER
113
REGISTER WRITE STAGE DATA REGISTER
116
fpc
101
ADDRESS INCREMENTER
102
0

FIG. 4


31 28 27 24 23 20 19 16 15 0
add dst, src1, src2
dst src1 src2 0000 0000 0000 0000 0000
load dst, (src1)
dst src1 0000 0001 0000 0000 0000 0000
store (src1), src2
0000 src1 src2 0010 0000 0000 0000 0000
jump src1
0000 src1 0000 0011 0000 0000 0000 0000
ext dst, src1, src2, code16
dst src1 src2 0100 code16

007260 "95th99960

FIG. 5

INPUTTED INSTRUCTION	OUTPUT					
bit 19~16	ALU CONTROL	dst NUMBER	dst VALID	FLUSH	ext VALID	CODE16
add 0000	01(add)	bit31~28	1	0	0	bit15~0
load 0001	00(nop)	bit31~28	1	0	0	bit15~0
store 0010	00(nop)	bit31~28	0	0	0	bit15~0
jump 0011	00(nop)	bit31~28	0	1	0	bit15~0
ext 0100	10(ext)	bit31~28	1	0	1	bit15~0

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007260 "95h99960

FIG. 6

ALU CONTROL INPUT	ALU OUTPUT
00 (nop)	SOURCE(1) REGISTER
01 (add)	SOURCE(1) REGISTER + SOURCE(2) REGISTER
10 (ext)	INPUT FROM EXTENDED ARITHMETIC UNIT

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FIG. 7

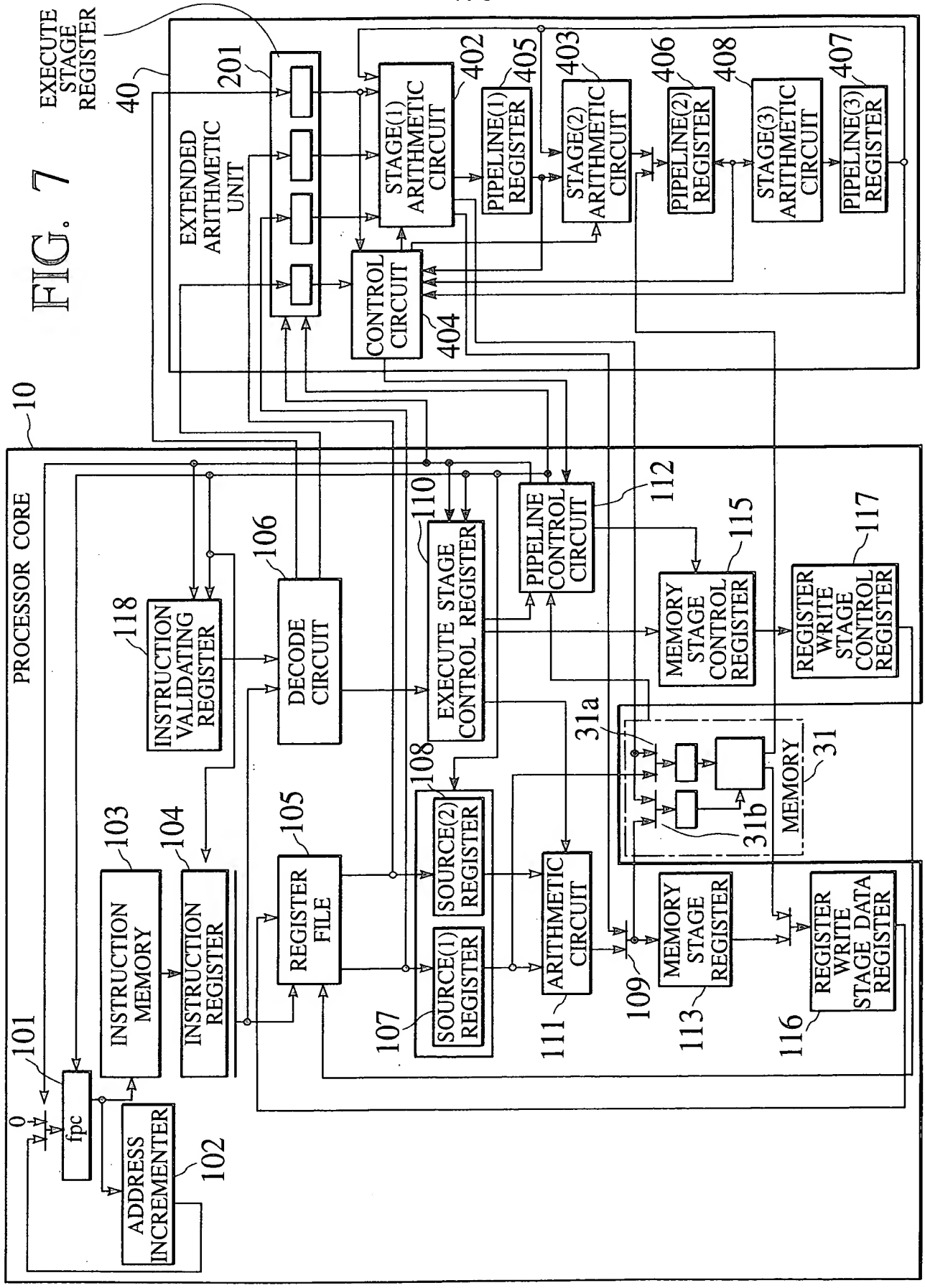
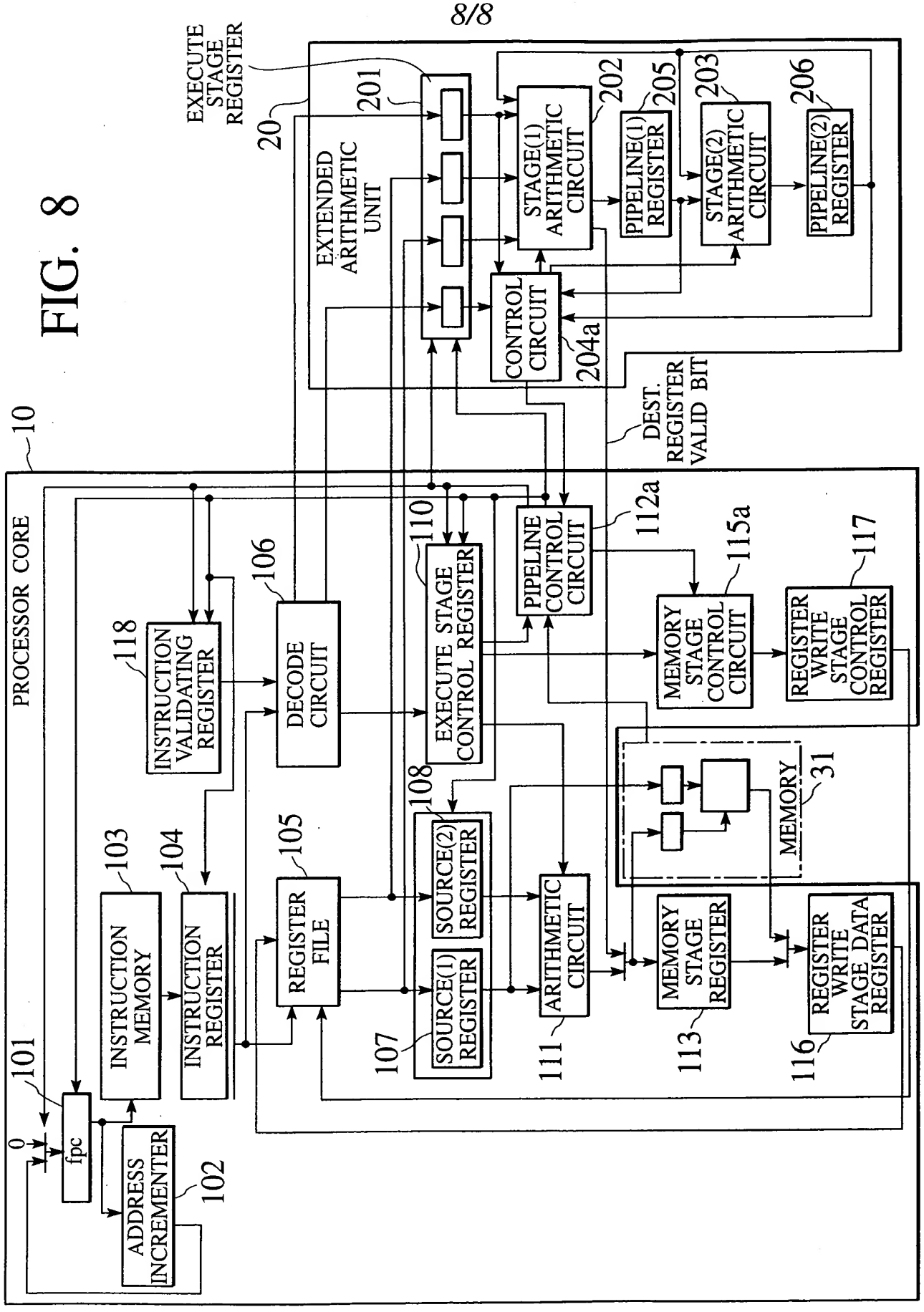

PROCESSOR CORE
10
EXECUTE STAGE REGISTER
40
EXTENDED ARITHMETIC UNIT
201
STAGE(1) ARITHMETIC CIRCUIT
402
PIPELINE(1) REGISTER
405
STAGE(2) ARITHMETIC CIRCUIT
403
PIPELINE(2) REGISTER
406
STAGE(3) ARITHMETIC CIRCUIT
408
PIPELINE(3) REGISTER
407
CONTROL CIRCUIT
404
INSTRUCTION VALIDATING REGISTER
118
DECODE CIRCUIT
106
EXECUTE STAGE CONTROL REGISTER
110
PIPELINE CONTROL CIRCUIT
112
MEMORY STAGE CONTROL REGISTER
115
REGISTER WRITE STAGE CONTROL REGISTER
117
31a
31b
MEMORY
31
INSTRUCTION MEMORY
103
INSTRUCTION REGISTER
104
REGISTER FILE
105
SOURCE(2) REGISTER
108
SOURCE(1) REGISTER
107
ARITHMETIC CIRCUIT
111
MEMORY STAGE REGISTER
109
113
REGISTER WRITE STAGE DATA REGISTER
116
fpc
101
0
ADDRESS INCREMENTER
102

FIG. 8


PROCESSOR CORE
10
EXECUTE STAGE REGISTER
20
EXTENDED ARITHMETIC UNIT
201
STAGE(1) ARITHMETIC CIRCUIT
202
PIPELINE(1) REGISTER
205
STAGE(2) ARITHMETIC CIRCUIT
203
PIPELINE(2) REGISTER
206
CONTROL CIRCUIT
204a
DEST. REGISTER VALID BIT
PIPELINE CONTROL CIRCUIT
112a
MEMORY STAGE CONTROL CIRCUIT
115a
REGISTER WRITE STAGE CONTROL REGISTER
117
EXECUTE STAGE CONTROL REGISTER
110
INSTRUCTION VALIDATING REGISTER
118
DECODE CIRCUIT
106
INSTRUCTION MEMORY
103
INSTRUCTION REGISTER
104
REGISTER FILE
105
SOURCE(2) REGISTER
108
SOURCE(1) REGISTER
107
ARITHMETIC CIRCUIT
111
MEMORY
31
MEMORY STAGE REGISTER
113
REGISTER WRITE STAGE DATA REGISTER
116
fpc
101
ADDRESS INCREMENTER
102
0